REMARKS

Claims 1-3, 10-13, 16-24, 26, 28-33 and 35-37 are pending. Claim 6 has been cancelled without prejudice or disclaimer.

I. CLAIM OBJECTIONS:

Claims 19-24, 26, 32-33 and 35-37 are objected to because of informalities. Claim 19 lines 5, 7, and 15-16 have been amended to reflect the Examiner's suggestions relating the correct usage of "a" and "the." Also, line 6 of claim 32 has been amended to recite "voltage; and" as suggested. Claim 36, line 3 now recites "a drain," as suggested. It is believed that these amendments address and overcome all of the noted objections.

II. CLAIM REJECTIONS 35 USC § 112:

Claims 10-13, 16-18 and 29-31 are rejected under 35 USC § 112, second paragraph as being indefinite. Claims 10-13 and 16-18 were rejected because the source/drain connections for the second and third transistors are reversed according to what one of ordinary skill would understand. Applicants have addressed this issue by amending claim 10 to reflect the proper connection. Claims 29-31 were rejected as being dependent upon a cancelled claim. Applicants have amended claim 29 to indicate dependency upon allowable claim 19. In light of these amendments, Applicants respectfully request the withdrawal of the rejections under 35 U.S.C. 112.

III. CLAIM REJECTIONS 35 USC § 103:

Hardee in view of Amanai

Claims 1-3, 6, 10-13, 15-18, 32-33 and 35-37 stand rejected under 35 USC 103(a) as being unpatentable over US 6,580,306 (Hardee) in view of US 6,128,230 (Amanai)[1]. This rejection is respectfully traversed as follows.

[1] To be thorough, further expedite prosecution, and for the sake of clarity, Applicants provide discussions of each of the references separately, however, Applicants are not attacking these references individually, but instead arguing that the references, even taken in combination, fail to render the claimed invention obvious because all features of the argued claim are not found in the prior art.

Fig. 1 of Hardee discloses a switching circuit 10 including PMOS transistor 12 having a thick gate insulation layer and NMOS transistors 14 and 16 having thin gate insulation layers. Transistor 12 is supplied by a first voltage VCCP. Transistors 14 and 16 are supplied with a second voltage VCC. The first voltage VCCP is greater than the second voltage VCC. An output, between transistors 12 and 14, is provided to an external circuit.

Claim 1 recites "an inverter coupled to a connection node of the first and third MOS transistors, the inverter driving a word line in a memory device." On page 6 of the Office Action, the Examiner asserts that it would have been obvious include such an inverter in the device of Hardee merely "if it was desired or required." Applicants submit that stating something is obvious simply because it may be desired does not establish a sufficient prima facie case of obviousness.

Even assuming that it would have been obvious to one of ordinary skill to include an inverter in the device of Hardee, which Applicants do not admit, Applicants respectfully submit that Examiner has not established a prima facie case of obviousness for stating that one of ordinary skill in the art would have been motivated to use an inverter having transistors with relatively thick gate oxides, as recited by amended claim 1. Claim 1 now requires an inverter "including NMOS and PMOS transistors having relatively thick gate insulation layers and operating at a third voltage higher than that of the power supply." Hardee does not disclose such a feature nor would it have been obvious to one of ordinary skill in the art to include this feature.

Fig. 1 of Amanai discloses a semiconductor memory device including a memory cell array, a main decoder, and a sub-decoder. The main decoder includes level shift circuits 15 and 16 having various NMOS and PMOS transistors and an inverter 14. However, Amanai does not address the thicknesses of the transistors' gate insulation layers for the inverter 14. Therefore, Hardee in view of Amanai, taken alone or in combination do not render claim 1 obvious.

Applicants submit that claim 1 is patentable for at least the foregoing reasons. Claims 2-3 are patentable at least by virtue of dependency upon claim 1.

Additionally, Applicants respectfully submit that claims 10 and 32 are patentable for reasons at least somewhat similar to those discussed above with regard to claim 1. Claims 11-13, 15-18, 33, and 35-37 are patentable at least by virtue of dependency upon claims 10 or 32.

Wright in view of Amanai

Claims 1-3, 6, 10-13, 16, 32-33 and 35-37 stand rejected under 35 USC 103(a) as being unpatentable over US 6,614,283 (Wright) in view of Amanai. Applicants traverse these rejections as follows.

Wright discloses a voltage level shifter that may transform an input signal of a first voltage to an output signal of a second voltage at an improved frequency. Fig. 2 depicts an example of such a device.

The Examiner asserts that Fig. 2 and column 4, lines 17-23, which indicate that transistor 208 has a medium or thick gate oxide, reads upon a second transistor having a relatively thin gate insulation layer, as required by claim 10. Although, Applicants do not agree with the Examiner's interpretation, claim 10 has been amended to recite that "the second and third transistors each have a relatively thin gate insulation layer, which are substantially the same thickness." Wright does not disclose or suggest at least this feature.

Fig. 1 of Amanai discloses a semiconductor memory device including a memory cell array, a main decoder, and a sub-decoder. The main decoder includes level shift circuits 15 and 16 having various NMOS and PMOS transistors. Amanai does not address the thicknesses of the transistors' gate insulation layers. Therefore, Wright in view of Amanai, taken alone or in combination, do not render claim 10 obvious.

Applicants submit that claim 10 is patentable over the cited art for at least the foregoing reasons. Claims 11-13 and 16 are patentable at least by virtue of dependency upon claim 10.

Additionally, Applicants respectfully submit that claims 1 and 32 are patentable for reasons at least somewhat similar to those discussed above with regard to claim 10. Claims 2-3, 33, and 35-37 are patentable at least by virtue of dependency upon claims 1 or 32.

CONCLUSION

In view of the above, Applicant earnestly solicits reconsideration and allowance of all of the pending claims.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,
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